# Machine-Verified <br> Network Controllers 

Nate Foster
Cornell University
frenetic >>

## Proof Assistants



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Arjun Guha
Postdoc $\rightarrow$ UMass


Mark Reitblatt
PhD student

## Networks in Practice



## Networks in Practice



## "The service outage was due to a series of internal network events that corrupted router data tables"

## Networks in Practice



## "The airline experienced a network connectivity issue..." <br> —United Airlines

## Networks in Practice



# "The airline experienced a network connectivity issue..." <br> —United Airlines 

Networks in Practice

There are hosts...

8
8
8

Networks in Practice

## Connected by switches...



Networks in Practice

There are also servers...


## Networks in Practice

Connected by routers...


Networks in Practice

And a load balancer...


## Networks in Practice

And a gateway router...


Networks in Practice

There are other ISPs...


Networks in Practice

## So we need to run BGP...



## Networks in Practice

And we need a firewall to filter incoming traffic...


## Networks in Practice

There are also wireless hosts...


## Networks in Practice

So we need wireless gateways...


## Networks in Practice

And yet more middleboxes for lawful intercept...


## Networks in Practice

## Each color represents a different set of control plane protocols and algorithms... this is



## Software-Defined Networking

A clean-slate architecture that standardizes features and decouples forwarding from


## Software-Defined Networking

## Essential ingredients

- Decouple control and data planes
- Logically-centralized control


## Enables

- Novel functionality
- Formal reasoning



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- Header Space Analysis [NSDI '12]
- VeriFlow [HotSDN '12]
- and many others...



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- and many others...

These are all great tools!
But they are expensive to run, and each builds on a custom (typically ad hoc) foundation


## Machine-Verified Controllers

## Vision

- Develop programs in a high-level language
- Reason at a high level of abstraction
- Use a compiler and run-time system to generate low-level control messages
- Machine-verified proofs of correctness


## Contributions

- NetCore compiler + optimizer
- Featherweight OpenFlow model
- General framework for establishing run-time system correctness



## OVERVIEW

## OpenFlow Switches



## H NOX

## Network Events

- Topology changes - Diverted packets
- Traffic statistics

Control Messages

- Modify rules
- Query counters


## Issue \#1: Switch-Level Errors

What happens if...
-The controller misses a keep-alive message?
-The controller sends a malformed message?

- Bad output port
- Too many actions
- Inconsistent actions
- Unsupported actions
-The switches runs out of space for rules?
Any of these can lead to essentially arbitrary behavior


## Issue \#2: Malformed Patterns

What happens if the controller sends the following message to a switch?

```
FlowMod AddFlow { match = { srcIPAddress = 10.0.1.*>, . .. },
    actions = [ flood ], ... }
```


## Issue \#2: Malformed Patterns

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We'd expect the switch to install a rule that broadcasts all traffic from a host the given subnet...

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Why? Switches silently ignore IP fields unless the Ethernet frame type is IP!

## Issue \#3: Message Reordering

What happens if the controller sends the following pair of OpenFlow messages to a switch in sequence?

```
FlowMod AddFlow { match = { ethFrameType = ethTypeIP,
                        srcIPAddress =
"10.0.1.99", ... },
    priority = 1,
    actions = [ ] }
FlowMod AddFlow { match = { ethFrameType = ethTypeIP,
    srcIPAddress = "10.0.1.*", ... },
    priority = 2,
    actions = [ flood ] }
```

The intention is to encode a negation...

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    priority = 2,
    actions = [ flood ] }
```

The intention is to encode a negation... ...but the switch may process these in either order!

## MACHINE-VERIFIED CONTROLLERS




## NetCore

## Syntax

Inductive pred : Type :=
(* Predicates *)
| OnSwitch : Switch -> pred
IngressPort : Port -> pred
DlSrc : EthernetAddress -> pred
DlDst : EthernetAddress -> pred
DlVlan : option VLAN -> pred
And : pred -> pred -> pred
Or : pred -> pred -> pred
| Not : pred -> pred
| All : pred
| None : pred.
Inductive PseudoPort : Type :=
PhysicalPort : Port -> PseudoPort AllPorts : PseudoPort.

Inductive act : Type :=
| FwdMod : Mod -> PseudoPort -> act
Inductive pol : Type :=
| Policy : pred -> list act -> pol
| Union : pol -> pol -> pol
| Restrict : pol -> pred -> pol.


Run-time system
$\downarrow$
OpenFlow messages

## NetCore

## Semantics

$$
\begin{gathered}
l p=(s w, p t, p k) \\
l p s_{\text {out }}=p o l(s w, p t, p k) \\
\frac{S=\left\{\left|\left(T\left(s w, p t_{\text {out }}\right), p k\right)\right|\left(p t_{\text {out }}, p k\right) \in l p s_{\text {out }}\right\}}{} \\
\left.\{\mid l p\} \uplus\left\{l p_{1} \cdots l p_{n}\right\} \xrightarrow{l p} S \uplus\left\{\mid l p_{1} \cdots l p_{n}\right\}\right\}
\end{gathered}
$$



- Models hop-by-hop forwarding behavior of the network
- Abstracts away from the underlying distributed system
- Makes it easy to reason about network-wide properties



## NetCore to Flow Tables

## Example

| Priority | Pattern | Action |
| :--- | :--- | :--- |
| 65534 | inPort $=2$, dlSrc $=\mathrm{dc}:$ ba $: 65: 43: 21$ | Fwd 2 |
| 65533 | inPort $=2$ | Fwd 3 |

## NetCore compiler

- Key operation: flow table intersection


Run-time system

```
OpenFlow messages
```

- Must restrict to "valid" patterns


## Optimizer

- Optimizer prunes (many) redundant rules
- Based on simple algebra of operations


## Correctness Theorem

## Valid Patterns

Inductive ValidPattern : Pattern -> Prop :=
| SupportedIPPatternValid : forall dlSrc dlDst dlVlan dlVlanPcp nwSrc nwDst nwTos tpSrc tpDst inPort nwProto,
In nwProto SupportedL4Protos ->
ValidPattern (MkPattern dlSrc dlDst (WildcardExact Const_0x800)
dlVlan dlVlanPcp
nwSrc nwDst (WildcardExact nwProto)
nwTos tpSrc tpDst inPort)
| UnsupportedIPPatternValid : forall dlSrc dlDst dlVlan dlVlanPcp nwSrc nwDst nwTos inPort nwProto,
~ In nwProto SupportedL4Protos ->
ValidPattern (MkPattern dlSrc dlDst (WildcardExact Const_0x800)
dlVlan dlVlanPcp
nwSrc nwDst (WildcardExact nwProto)
nwTos WildcardAll WildcardAll inPort)
| ARPPacketValid : forall dlSrc dlDst dlVlan dlVlanPcp nwSrc nwDst inPort, ValidPattern (MkPattern dlSrc dlDst (WildcardExact Const_0x806)
dlVlan dlVlanPcp
nwSrc nwDst WildcardAll
WildcardAll WildcardAll WildcardAll inPort)
UnknownDlTypPatternValid : forall dlSrc dlDst dlTyp dlVlan dlVlanPcp inPort, ValidPattern (MkPattern dlSrc dlDst dlTyp
dlVlan dlVlanPcp
WildcardAll WildcardAll WildcardAll
WildcardAll WildcardAll WildcardAll inPort)
| EmptyPatternValid : ValidPattern Pattern_empty.


Featherweight OpenFlow

## OpenFlow Specification

| F |  | $\overline{7}$ |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| － | ＝ | E |  |  |  |  |
|  |  |  |  |  |  |  |
| E |  | － |  |  | $=$ |  |
| \＃ |  | 钲 |  |  |  |  |
|  |  |  |  |  |  |  |
| 曾 |  | 家 |  |  |  |  |
|  |  | ＝ |  |  | E |  |
| T |  | E |  |  |  |  |
| \＃ |  |  |  |  |  |  |

42 pages．．．
．．．of informal English text
．．．and C struct definitions

## Featherweight OpenFlow

## Syntax



## Key judgments:

- Controller in:
$(s w, C M, \sigma) \rightsquigarrow \sigma^{\prime}$
- Controller out: $\sigma \rightsquigarrow\left(s w, S M, \sigma^{\prime}\right)$
- Network step: $\quad M \rightarrow M^{\prime}$

Models all essential asynchrony

## Semantics

$\mathbb{S}(s w, p t s, R T,\{l p \mid\} \uplus$ inp, outp, inm, outm $) \xrightarrow{l p} \mathbb{S}\left(s w, p t s, R T\right.$, inp, outp $p^{\prime} \uplus$ outp, inm, outm ${ }^{\prime} \uplus$ outm $)$
(Ркт-Process)
$\longrightarrow \mathbb{S}(s w, p t s, R T$, inp,$\{((s w, p t, p k)\} \uplus$ outp, inm, outm $) \mid \mathbb{L}((s w, p t), p k s$, loc' $)$ (Send-Wire)
$\rightarrow \mathbb{S}(s w, p t s, R T$, inp, outp, inm, outm $) \mid \mathbb{L}\left((s w, p t),[p k]+p k s, l o c{ }^{\prime}\right)$
$\mathbb{L}(l o c, p k s+[p k],(s w, p t)) \mid \mathbb{S}(s w, p t s, R T$, inp, outp, inm, outm) (RECV-WIRE)
$\xrightarrow{(s u, p t, p k)} \mathbb{L}(l o c, p k s,(s w, p t)) \mid \mathbb{S}(s w, p t s, R T,\{(s w, p t, p k)\} \uplus$ inp, outp, inm, outm $)$
$\frac{R T^{\prime}=\operatorname{apply}(\Delta R T, R T)}{\frac{\mathbb{S}(s w, p t s, R T, \text { inp }, \text { outp },\{\text { FlowMod } \Delta R T\} \uplus \text { inm }, \text { outm }) \longrightarrow \mathbb{S}\left(s w, p t s, R T^{\prime}, \text { inp, outp }, \text { inm, outm }\right)}{\text { (SwITCH-FLowMod) }}}$
$\overline{\mathbb{S}(s w, p t s, R T, \text { inp, outp, }\{\text { PktOut } p t p k \mid\} \uplus \text { inm, outm }) \longrightarrow \mathbb{S}(s w, p t s, R T, \text { inp },\{(s w, p t, p k)\} \uplus \text { outp }, \text { inm }, \text { outm })}$ (Switch-РктOut)
$\frac{f_{\text {out }}(\sigma) \rightsquigarrow\left(s w, S M, \sigma^{\prime}\right)}{\mathbb{C}\left(\sigma, f_{\text {in }}, f_{\text {out }}\right)\left|\mathbb{M}(s w, S M S, C M S) \longrightarrow \mathbb{C}\left(\sigma^{\prime}, f_{\text {in }}, f_{\text {out }}\right)\right| \mathbb{M}(s w,[S M]+S M S, C M S)}$ (CTRL-SEND)
$\frac{f_{\text {in }}(s w, \sigma, C M) \rightsquigarrow \sigma^{\prime}}{\mathbb{C}\left(\sigma, f_{\text {in }}, f_{\text {out }}\right)\left|\mathbb{M}(s w, S M S, C M S+[C M]) \longrightarrow \mathbb{C}\left(\sigma^{\prime}, f_{\text {in }}, f_{\text {out }}\right)\right| \mathbb{M}(s w, S M S, C M S)}$ (CtrL-RECv)
$S M \neq$ BarrierRequest $n$
$\mathbb{M}(s w, S M S+[S M], C M S) \mid \mathbb{S}(s w, p t s, R T$, inp, outp, inm, outm) (Switch-Recv-CtrL)
$\longrightarrow \mathbb{M}(s w, S M S, C M S) \mid \mathbb{S}(s w, p t s, R T$, inp, outp,$\{\mid S M\} \uplus$ inm, outm $)$
$\mathbb{M}(s w, S M S+[$ BarrierRequest $n], C M S) \mid \mathbb{S}(s w, p t s, R T$, inp, outp, $\emptyset$, outm $)$
$\longrightarrow \mathbb{M}(s w, S M S, C M S) \mid \mathbb{S}(s w, p t s, R T$, inp, outp $, \emptyset,\{$ BarrierReply $n\} \uplus$ outm $)$ (Switch-Recv-Barrier)

[^0]

## Run-Time System

## Invariants

- Maintain a sound approximation of overall flow table each switch
-Eventually process all diverted packets


## Theorem



FlowTable $\approx$ Featherweight OpenFlow

## Run-time instances

- Trivial: processes all packets on controller
- Proactive: installs rules, falls back to Trivial when out of space
- Full: like Proactive, but also installs exact-match rules


## Safe Wires

```
Inductive SafeWire : SF -> SF -> SF -> list CM -> Prop :=
| SafeWire_nil : forall lb ub,
        extends ub lb ->
        SafeWire lb ub lb nil
    | SafeWire_cons_FlowMod : forall lb ub sf sft lst,
        SafeWire lb ub sf lst ->
        extends ub (apply_SFT sft sf) ->
        SafeWire lb ub (apply_SFT sft sf) (FlowMod sft :: lst)
    | SafeWire_cons_PktOut : forall lb ub sf pt pk lst,
        SafeWire lb ub sf lst ->
        SafeWire lb ub sf (PktOut pt pk :: lst)
    | SafeWire_cons_BarrierRequest : forall lb ub sf n lst,
        SafeWire lb ub sf lst ->
        SafeWire lb ub sf (BarrierRequest n :: lst).
```


## Implementation

## Source

- ~8,000 lines of Coq
- 1,500 lines of Haskell


## Components

- NetCore compiler and optimizer
- Flow tables
- Featherweight OpenFlow
- Run-time system instances
- Proofs of correctness


## Status

- Extracts to Haskell source code
- Compiles against Nettle libraries
- Running on "production" traffic in the lab


## Performance

- Unverified
$\square$ Verified
5,000



## Conclusion

Networks are critical infrastructure...
...developed using 1970s-era techniques


Software-defined networks are an networks on a solid foundation

Machine-verified controllers based on NetCore a first step in this direction

## A Grand Collaboration: Languages + Networking

Frenetic Cornell
Shrutarshi Basu (PhD)
Nate Foster (Faculty)
Arjun Guha (Postdoc)
Stephen Gutz (Undergrad)
Mark Reitblatt (PhD)
Robert Soulé (Postdoc)
Alec Story (Undergrad)

## Frenetic Princeton

Chris Monsanto (PhD)
Joshua Reich (Postdoc)
Jen Rexford (Faculty) Cole Schlesinger (PhD)
Dave Walker (Faculty)
Naga Praveen Katta (PhD)

# frenetic >> 

http://frenetic-lang.org


[^0]:    $\mathbb{S}(s w, p t s, R T$, inp, outp, inm, $\{C M\} \uplus$ outm $) \mid \mathbb{M}(s w, S M S, C M S)$ (SWITCH-SEND-CTRL)
    $\longrightarrow \mathbb{S}(s w, p t s, R T$, inp, outp, inm, outm $) \mid \mathbb{M}(s w, S M S,[C M]+C M S)$

