Designing Correct Circuits 2010

A Satellite Workshop of ETAPS'10

Paphos, Cyprus, 20-21 March 2010

CALL FOR ABSTRACTS

Abstracts due: **Monday 7 December November 2009**
Notification of acceptance: Monday 21 December 2009
Final version: Wednesday 20 January 2010

A two-day workshop on the topic Designing Correct Circuits will be held on 20-21 March 2010 in Paphos, Cyprus, as part of the ETAPS group of conferences. The workshop will bring together researchers in formal methods for hardware design and verification from academia and industry. It will allow participants to learn about the current state of the art in formally-based hardware design and verification, and is intended to spark debate about how more effective verification methods can be developed. Much research in these areas now takes place in industry, rather than in academia. For the long term survival of our field, we must ensure that academics and industrial researchers continue to work together on the real problems in correct circuit design and verification, including those currently being faced in microprocessor design, System-on-a-Chip development, and in the automotive and aerospace industries.

A major aim of this workshop is to strengthen the existing communication channels and to open more of them. The DCC workshops have been held biennially since 2002 and have always been a great success in creating an informal forum where these issues could be discussed. We hope for something similar in 2010.

This call invites you to submit a one page description of a talk that you would like to give at this workshop. One page abstracts of your talks can be submitted to Joe Stoy (`stoy@bluespec.com`) by 23 November 2009.

The abstract should describe original work, and should indicate what distinguishes your work from other research on languages for and approaches to the design and verification of hardware. Describe the status of your work such as, for example, industrial experience with conclusions, new idea with prototype implementation, new theory, comparison of methods, etc. Please indicate clearly how your talk will contribute to the kind of debate that we are hoping to generate. Include a list of references on a second page if you wish. Researchers from both industry and academia are encouraged to submit talks. Speakers from industry who would be willing to present research problems that they face (and with which they need help) would also be welcome. We would like to be able to present a broad view of the current state of the art in design and verification methods.

The final programme will be agreed by the workshop committee no later than 21 December 2009, and a final version of the material for the participants proceedings will be due on 20 January 2010. This would preferably be a draft paper, but could also be slides. The workshop speakers and the workshop committee will decide after the workshop whether or not to make a more permanent record, for example by arranging a special issue of a journal.

Workshop Committee

Arvind (MIT)
Per Bjesse (Synopsys)
Wolfgang Kunz (University of Kaiserslautern)
Bob Kurshan (Cadence)
Pete Manolios (Northeastern University)
Andy Martin (IBM)
Tom Melham (University of Oxford)
Gordon Pace (University of Malta)
Marc Pouzet (University of Paris-Sud)
Carl Seger (Intel)
Satnam Singh (Microsoft)
Joe Stoy (Bluespec)

Contact:

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